A 10b 700MS/s single-channel 1b/cycle SAR ADC using a monotonic-specific feedback SAR logic with power-delay-optimized unbalanced N/P-MOS sizing

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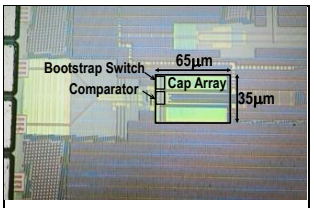
A SAR ADC comprises only a T/H, a comparator, SAR logics, and a capacitive DAC, thus exhibiting a power-efficient topology with low complexity, low power consumption, and friendly process technology scaling down. Consequently, it has a wide utilization in high-speed applications (like in time-interleaved SARs). Previous works improved the 1b/cycle topology to speed up SAR ADC conversions, leading to multi-bit/cycle [1] and N-bits N-comparators [2] structures. Compared with the above architectures, the conventional 1b/cycle topology still has apparent advantages related to low complexity, less parasitic, and less offset problems. Therefore, currently, the 1b/cycle is still the first choice for the majority of high-speed TI SAR ADCs [3]. The popularization of the high-speed SAR ADC with redundant bit structures can lead to a very short settling time required for the DACs [4]. However, the speed of the SAR is still a bottleneck, especially limited by the digital SAR logic [2].

This work proposes a power-delayed-optimized SAR feedback loop composed of unbalanced N/P-MOS sizing, reducing the SAR logic delay to overcome the single-channel SAR ADC's speed bottleneck. Based on the characteristics of the commonly used monotonic-switching SAR ADC [4] that switches the DAC in only a single direction, we can reduce the comparator-to-DAC delay by sizing the N/P-MOS of the logic gates unilaterally (Fig. 1) along the path of the monotonic switching DAC drivers, the DAC switch control logic, and the asynchronous control logic. The proposed technique enhances the speed of the logic on those critical edge transitions, and reduces the size of the transistors for those non-critical edge directions. This can simultaneously improve the speed, and reduce the power and area of the SAR ADC, breaking the traditional power-delay tradeoffs of the SARs. Furthermore, it does not change the classic 1b/cycle structure, which allows all its advantages to be maintained.

The monotonic switching SAR ADC [4] resets the bottom plates of all DAC capacitors to VDD in the sampling phase. The subsequent switching of each bit's capacitor bottom plate to GND (critical edge direction) or keeping it unchanged at VDD (non-critical edge direction) depends on the comparator's digital output (OUTP/OUTN) and the corresponding internal SAR clocks (CLK_i). From Fig. 1, the speed-critical edge direction for the i-th bit capacitor's bottom plate (C_i) is always the falling edge in the monotonic switching DAC. Thus, we can determine that the rising edge is the critical direction for the corresponding DAC switch control signal (DAC_i). Similarly, the corresponding critical direction for the asynchronous control clocks (CLK_i) must be from 0 to 1, with all DFFs in the asynchronous control logic reset in the sampling phase. In summary, speed-critical edges from the capacitor's bottom plate C_i to the DAC drivers, the DAC switch control signal DAC_i, and the asynchronous control clocks CLK_i are definite and unidirectional.

Under normal circumstances, we use N/P-MOS g_m-balanced digital buffers to drive the switch control signals of the DAC. This can ensure symmetrical rising and falling edges of the digital buffers with similar delays. However, for the logic drivers of the monotonic switching DAC, they are unidirectional in each conversion cycle. It means that we only need to optimize the corresponding unilateral direction of the data transmission. Fig. 2 presents the fast one-sided digital buffer in the driver circuits of the monotonic switching DAC, composed of the un-balanced N/P-MOS. In the conversion phase, the node 'OUT', which is the bottom plate of C_i, switches to either the GND or does not change. Therefore, the speed-critical edges in the nodes 'OUT/C/B/A' are always falling/rising/falling/rising edges, respectively.

From Fig.2, in the traditional digital buffer, the ratio of the widths of NMOS (M_{N1}, M_{N2}, M_{N3}, M_{N4}) to PMOS (M_{P1}, M_{P2}, M_{P3}, M_{P4}) is approximately equal to the mobility ratio of PMOS and NMOS, such as $W_{P2}\approx(\mu_N/\mu_P)W_{N2}$, $W_{N3}\approx(\mu_P/\mu_N)W_{P3}$. The proposed power-delay-optimized digital buffer reduces the corresponding widths of NMOS or PMOS transistors by a shrink factor $\alpha<1$, like $W_{N1}\approx(\mu_P/\mu_N)\alpha W_{P1}$, $W_{P2}\approx(\mu_N/\mu_P)\alpha W_{N2}$. The utilization of the shrink factor α for W_{P2} reduces $C_{L,A}$ when compared with the traditional buffer; the delay time becomes $T_{delay\text{-}proposed}\approx(1+\alpha)/2\cdot T_{delay\text{-}regular}$. Moreover, each node of the logic path's capacitive load and the power consumption fall by a factor of (1+α)/2.



Die micrograph.

We can extend this concept to other digital logic circuits, such as NAND, NOR, the logic gates in the DFFs, etc., by using unbalanced N/P-MOS sizing to reduce delay and power consumption. We can set the actual value of 'α' differently for different logic locations. Fig. 3 displays how to use the proposed method to optimize the delay in a monotonic switching SAR according to specific situations. There are 3 critical delay paths for the SAR logic loop. Path 1 (red in Fig. 3) controls the strobe and reset of the comparator during the conversion phase. Both the rising and falling edges in this path are critical for the speed of SAR conversion phase, so we use traditional regular-sizing logic within this path 1. From the 'Ready' signal generated based on the output of the comparator to the asynchronous control clock CLK_i (path 2, blue), then to the DAC switch control logic DAC_i and the bottom plates of C_i (path 3, brown), we intentionally place the non-critical edges in the sampling phase and the critical edges in the SAR conversion phase. Considering the CLK_i as an example, they have more than the time of the entire sampling phase to complete the non-critical edge transitions (reset) without affecting the performance of the ADC. α can be as small as possible (between 0.1 and 0.25 here). In the SAR logic feedback loop, registers such as DFFs generally occupy the main part of the delay time and power. Using the proposed unbalanced N/P-MOS sizing method, we re-optimize the DFF's design. On one hand, we reduce the number of gates required for the critical propagation path in the DFF. On the other hand, using unbalanced logic further reduces the critical path delay. For path 3 from DAC_i to C_i, it is necessary to pay attention to the reset of C_i while performing unilateral optimization. The slowest reset of C_i will affect the sampling accuracy of the ADC. In this work, we use the sampling clock 'Φ_S' to reset DAC_i directly. In the path from DAC_i to C_i, we choose α from 0.25 to 0.5 to improve the one-way high-speed propagation during the conversion phase while maintaining the moderate reset capability of the DAC in sampling phase. Finally, the unbalanced N/P-MOS sizing method reduces the total capacitive loads along the paths. An important consequence is the significant reduction of the number of buffer stages to drive them. Therefore, it contributes to a further reduction of the logic delay and the power.

To verify the proposed power-delay-optimized unbalanced N/P-MOS sizing technique, we fabricated a 10-bit SAR ADC in 28nm CMOS. This 10-bit SAR ADC has 11 cycles (1bit redundant), the first two MSBs use a monotonic splitting structure, and the remaining bits are pure monotonic. We used a custom-designed MOM capacitor array with a total single-ended ADC input capacitance of 180fF to deliver a 10b-level INL of -0.51/+0.60 LSB. It achieves the Nyquist SNDR/SFDR of 56.39/71.95dB at 600MS/s @0.9V, and 56.42/73.27dB at 700MS/s @0.95V (Fig. 4). Fig. 5 presents the robustness measurement, including the dynamic performance versus supply voltage, different chip samples, and ambient temperature. Fig. 6 compares the performance with recently published ADCs of similar performance.

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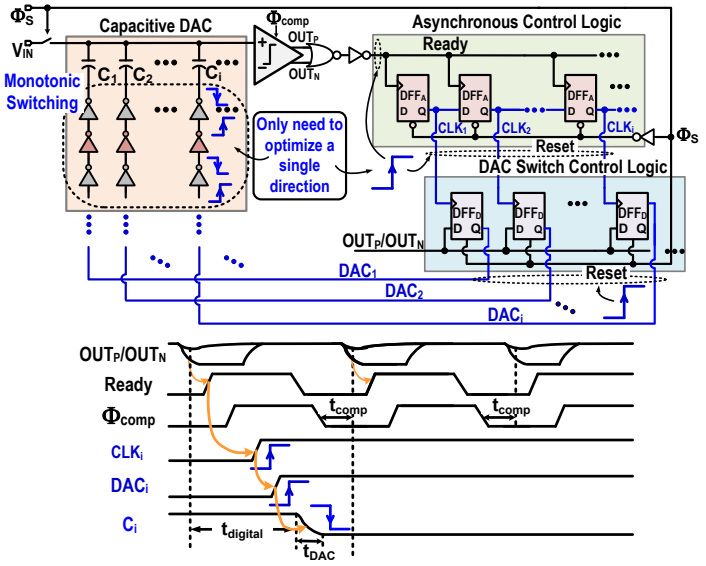

Fig. 1. Unidirectional data transmission path in monotonic switching SAR ADC.

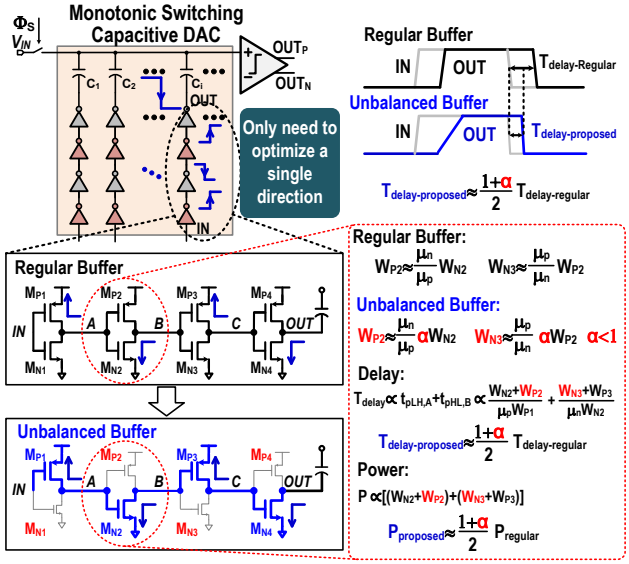

Fig. 2. Proposed power-delay-optimized unbalanced N/P-MOS sizing buffer.

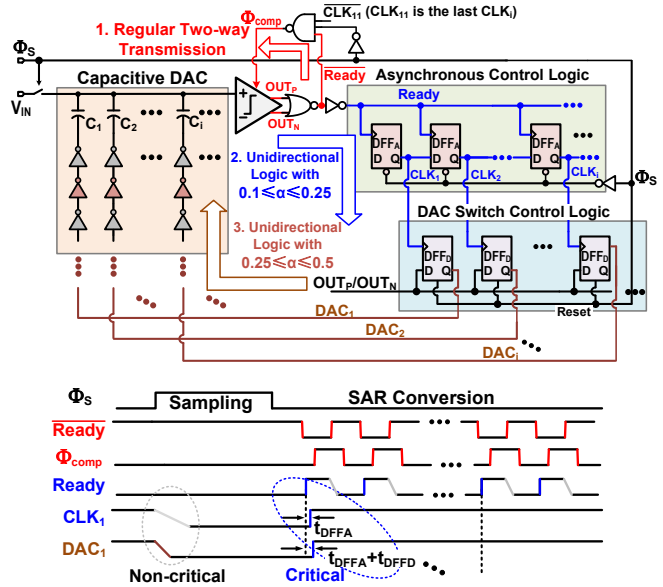

Fig. 3. Optimization of 3 delay paths in monotonic switching SAR.

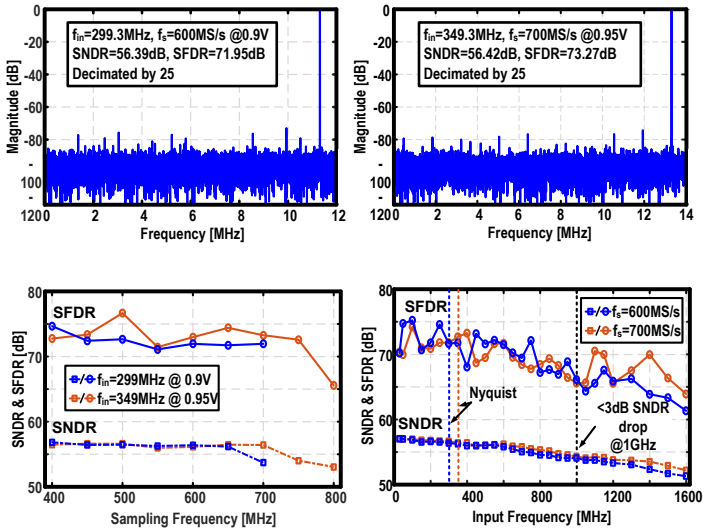

Fig. 4. Measured 16384-point output spectrum with a sampling rate of 600MS/s @0.9V and 700MS/s @0.95V, measured performance vs. sampling frequencies and input frequencies.

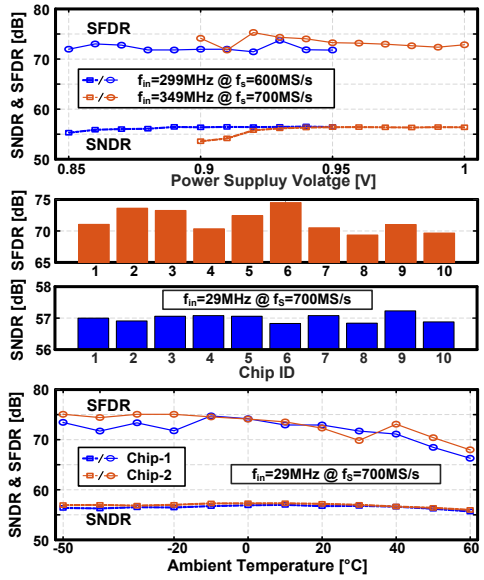

Fig. 5. Measured SNDR & SFDR vs supply, samples, temperature.

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Architecture	SAR		SAR		Pipe-SAR		Pipe	Pipe-SAR-DSM	Pipe-SAR	
Calibration Free	√		√		×		×	×	×	
Process	28nm		20nm		14nm		16nm	7nm	16nm	
Resolution [bit]	10		10		10		11	12	12	
Supply Volatge	0.9	0.95	0.9	1	0.7	0.95	0.85	0.8	0.9	
Sampling Rate [MS/s]	600	700	160	320	950	1500	600	600	500	
SNDR @ Nyq. [dB]	56.39	56.42	57.1	50.7	50.3	50.1	60.2	55.3	62.9	62.3*
Power [mW]	1.49	2.02	0.68	1.52	2.26	6.92	6	13	2.8	3.3*
FOM_{Walden} [fJ/c-s]	4.6	5.3	7.3	16.5	8.9	17.7	12	45.6	4.9	6.2*
$FOM_{Schreier}$ [dB]	169.4	168.8	167.8	160.9	163.5	160.4	167.2	158.9	172.4	171.1*
Active Area [mm²]	0.0023		0.0012		0.0016		0.037	0.037	0.0084	

*: Reference regulation on.

Fig. 6. Performance summary and comparison with state-of-the-art.